

FIG. 1

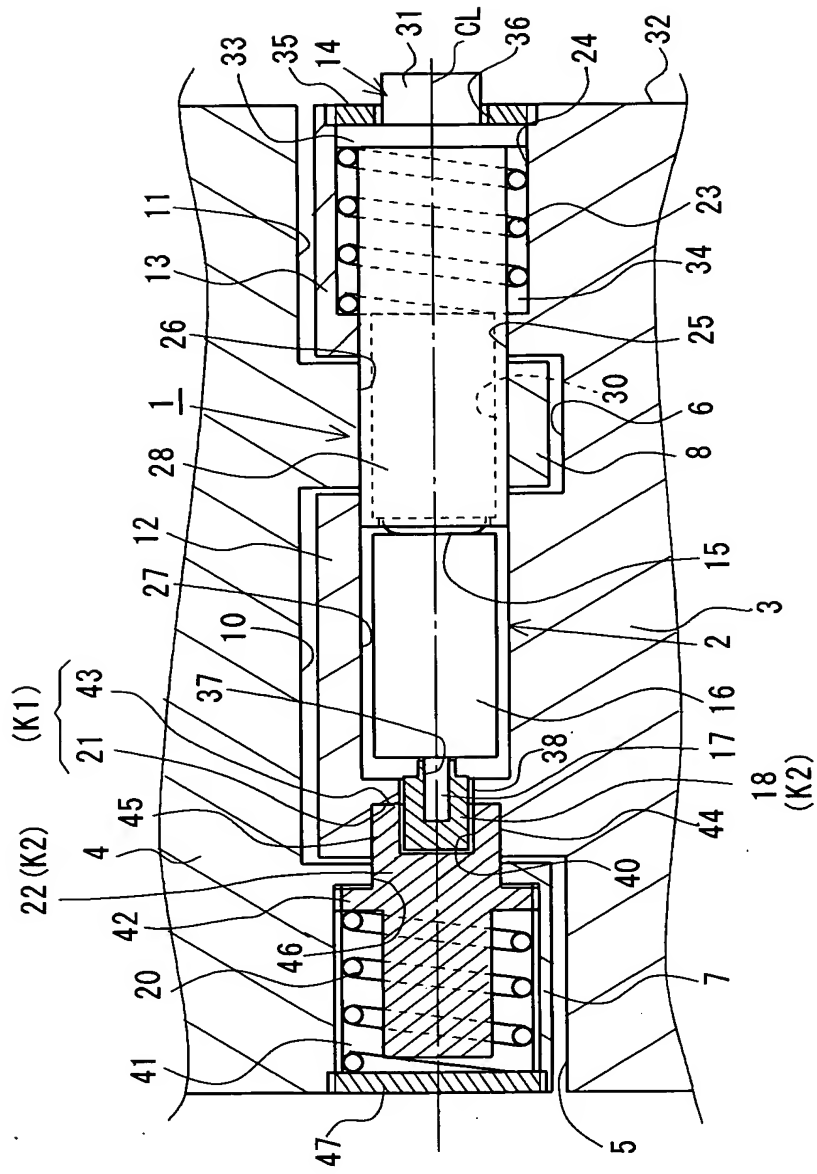


FIG. 2

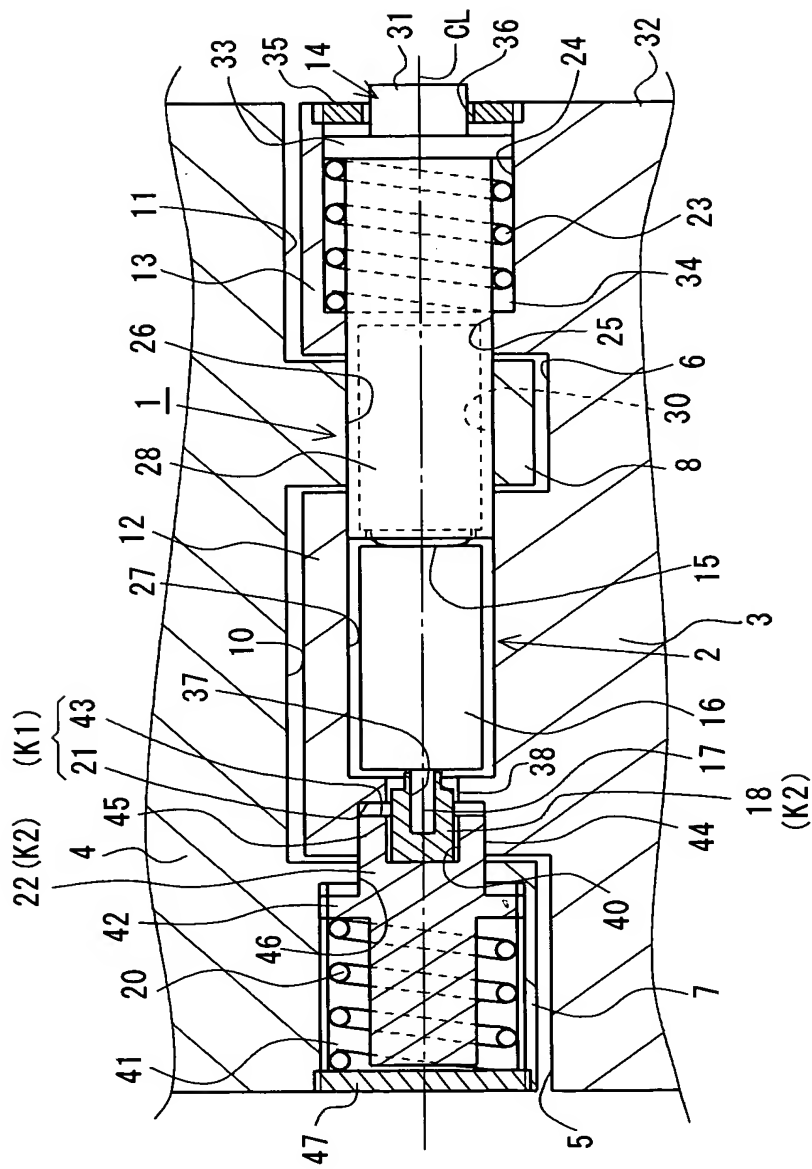


FIG. 3

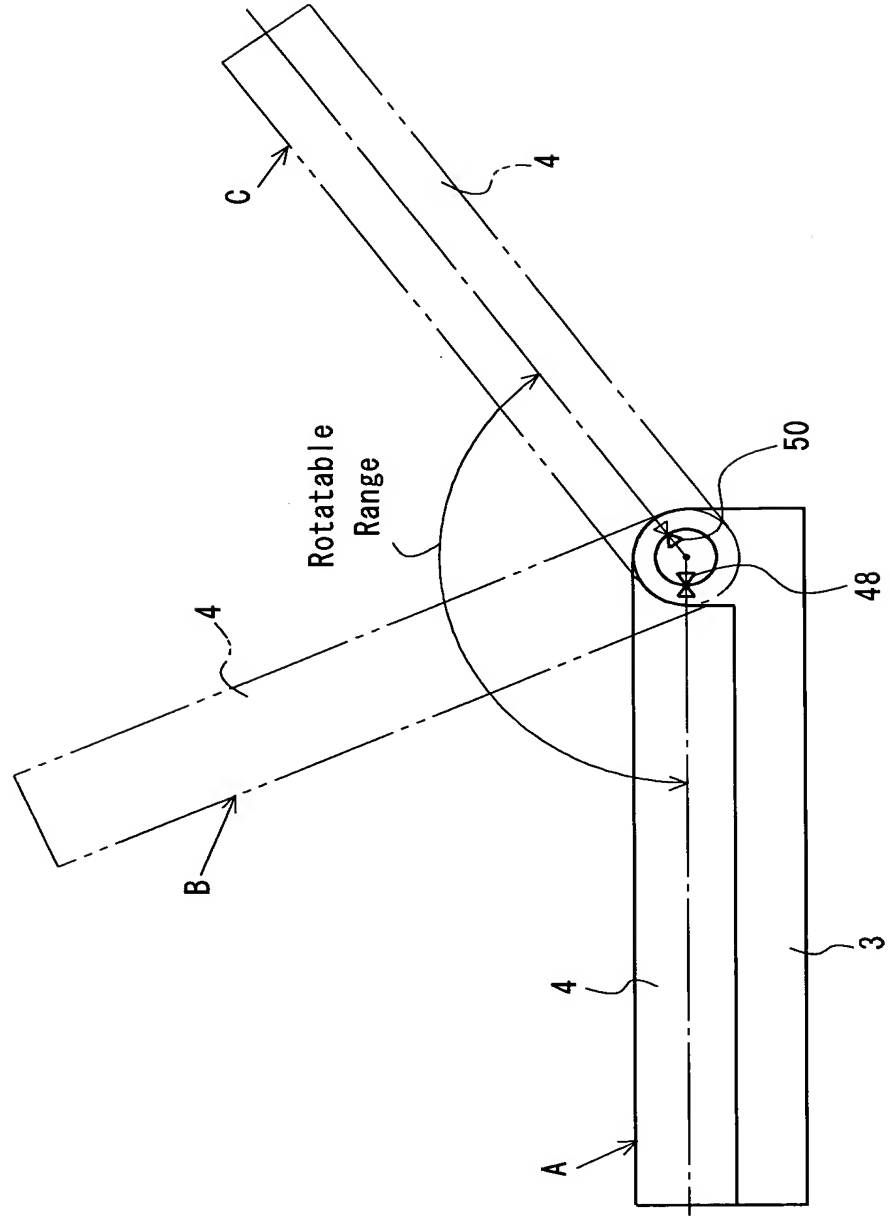


FIG. 4

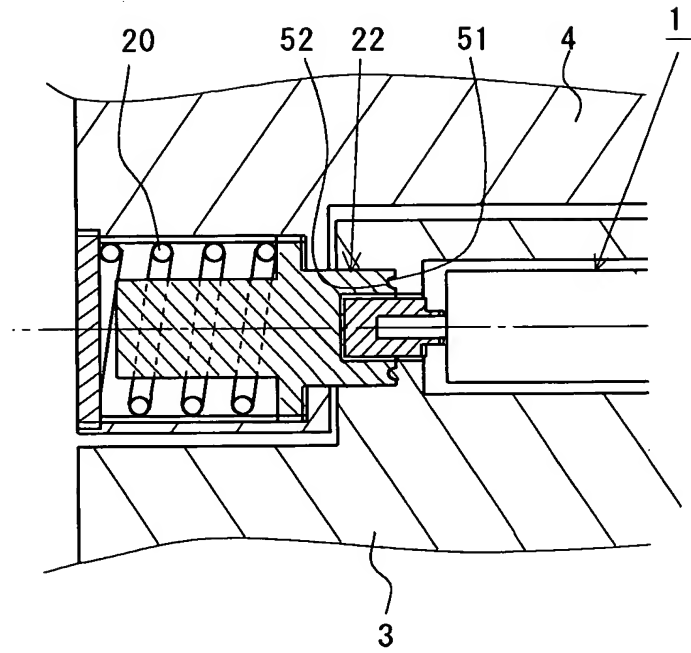


FIG. 5

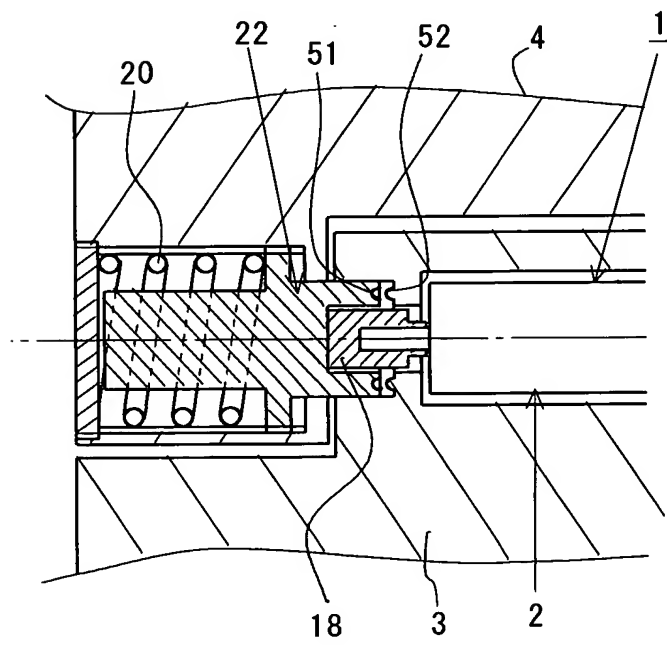


FIG. 6A

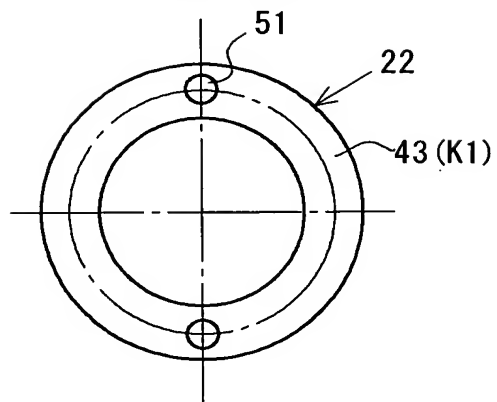


FIG. 6B

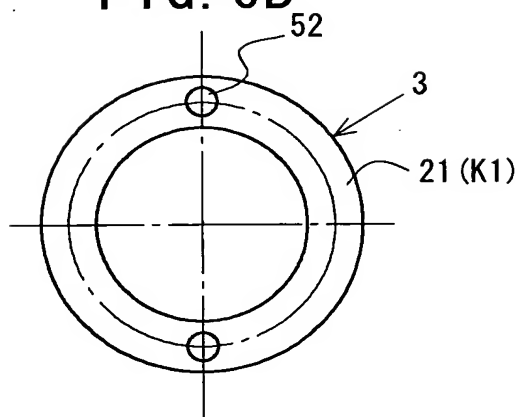


FIG. 7A

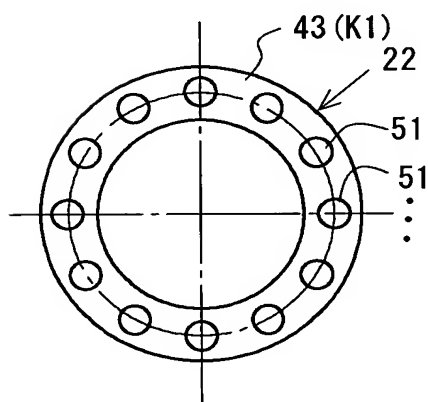


FIG. 7B

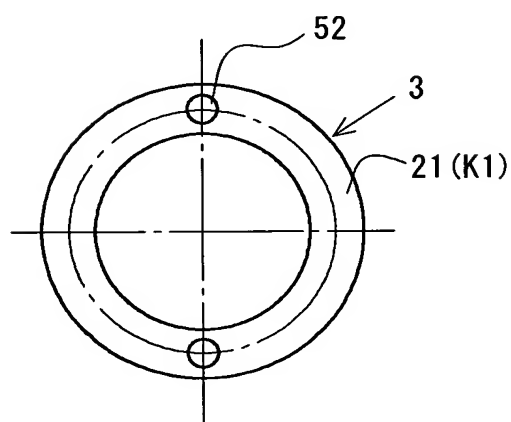


FIG. 8A

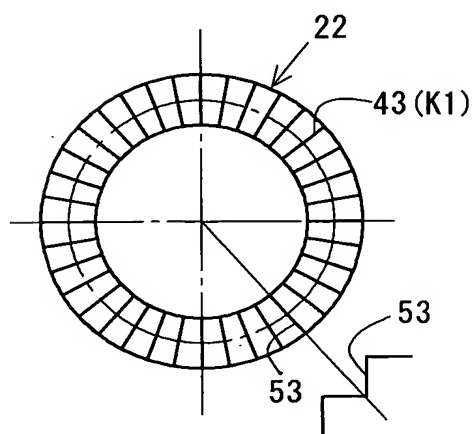
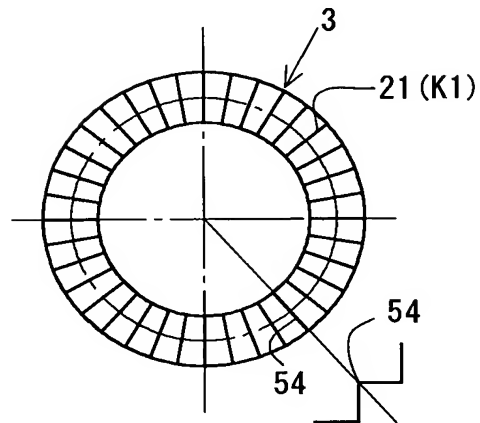
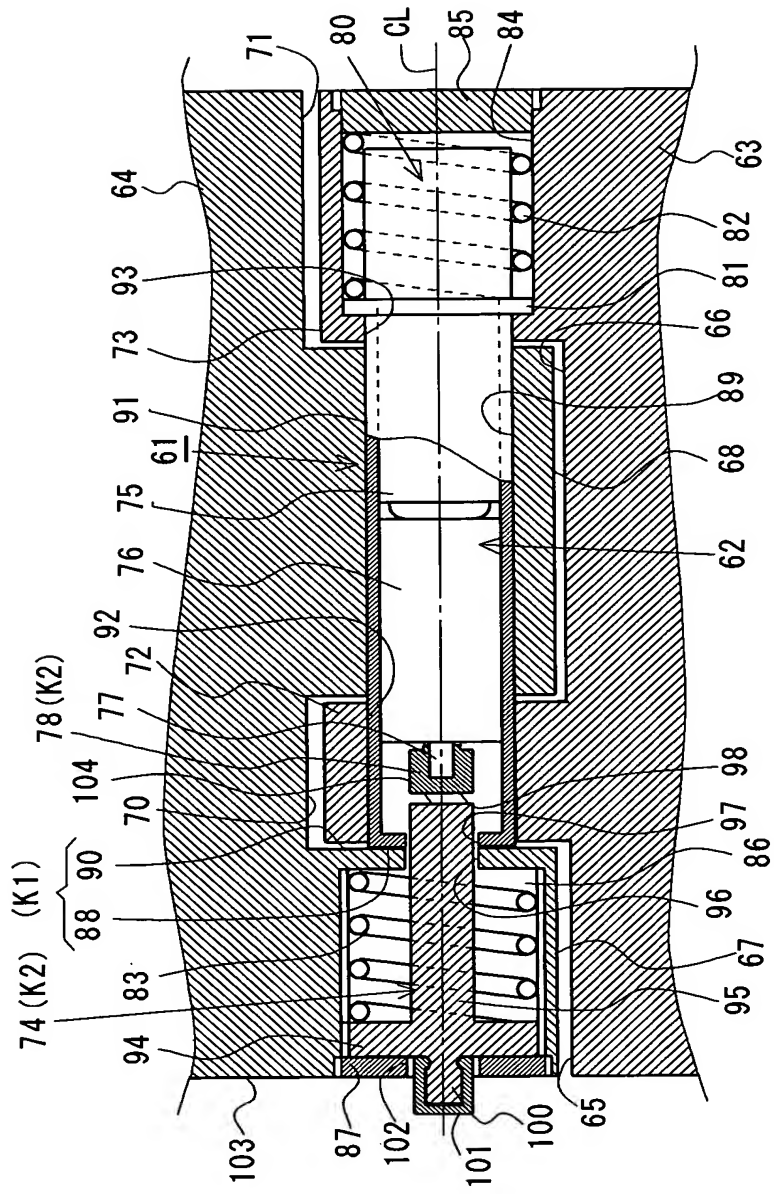


FIG. 8B





This diagram shows a cross-section of a semiconductor device. It features a central channel region (CL) defined by a gate stack (80). The channel is flanked by source and drain regions (71, 72). Various layers are labeled, including 103, 87, 102, 101, 100, 65, 94, 83, 74(K2), 88, 90, 78(K2), 104, 70, 77, 92, 76, 75, 61, 91, 73, 93, 64, 62, 68, 89, 66, 81, 82, 63, 95, 67, 96, 86, 97, 98, 62, 68, 89, 66, 81, 82, 63, 95, 67, 96, 86, 97, 98. A dashed line indicates the center of the channel.

FIG. 11

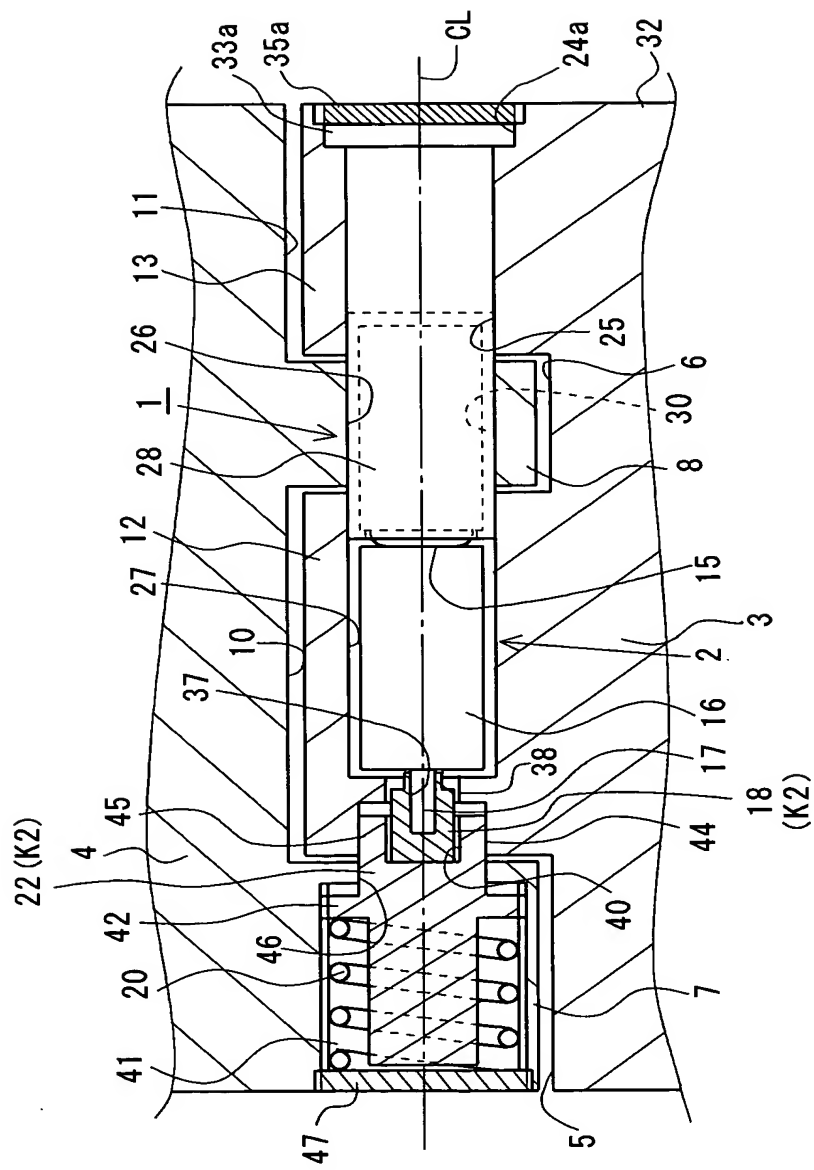


FIG. 12

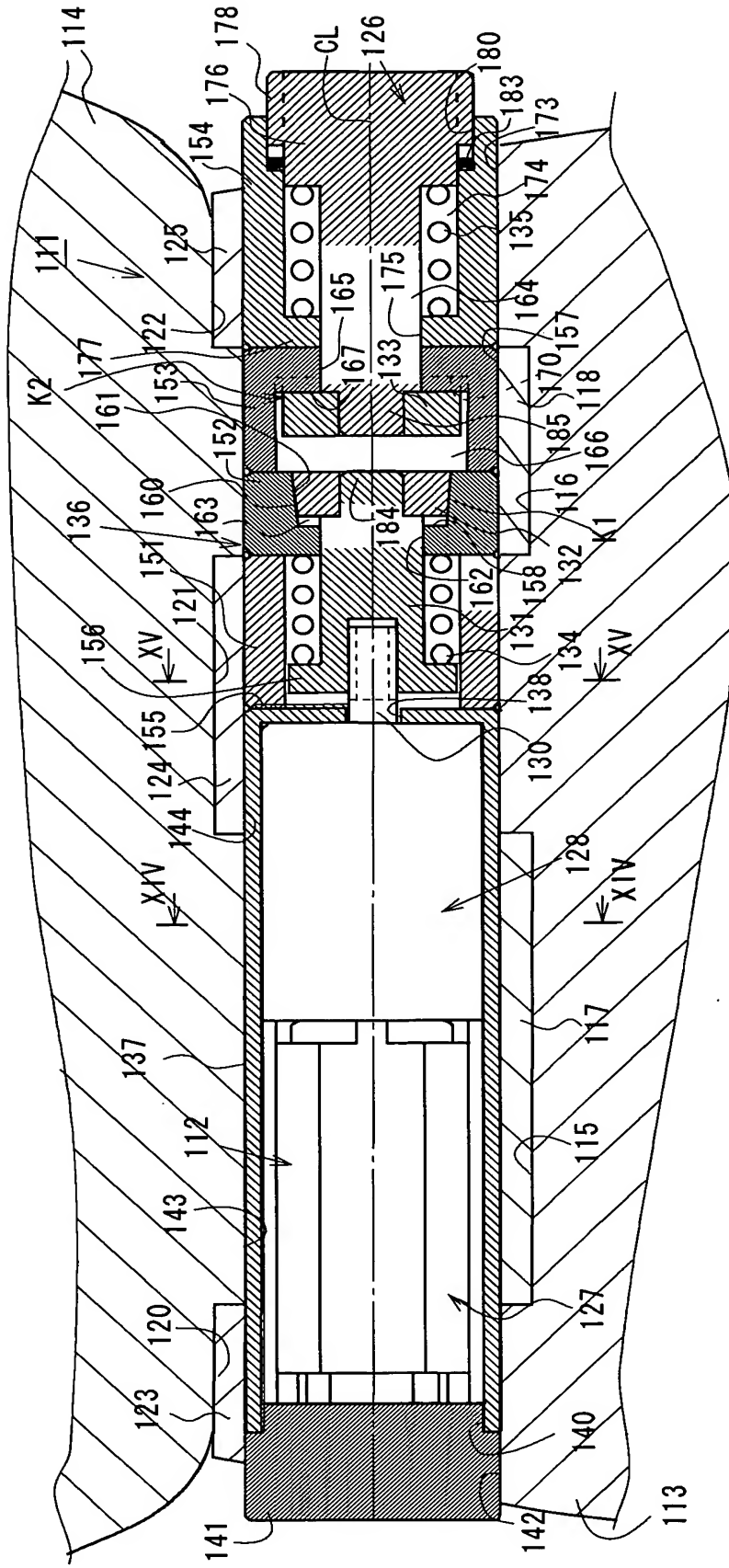


FIG. 13

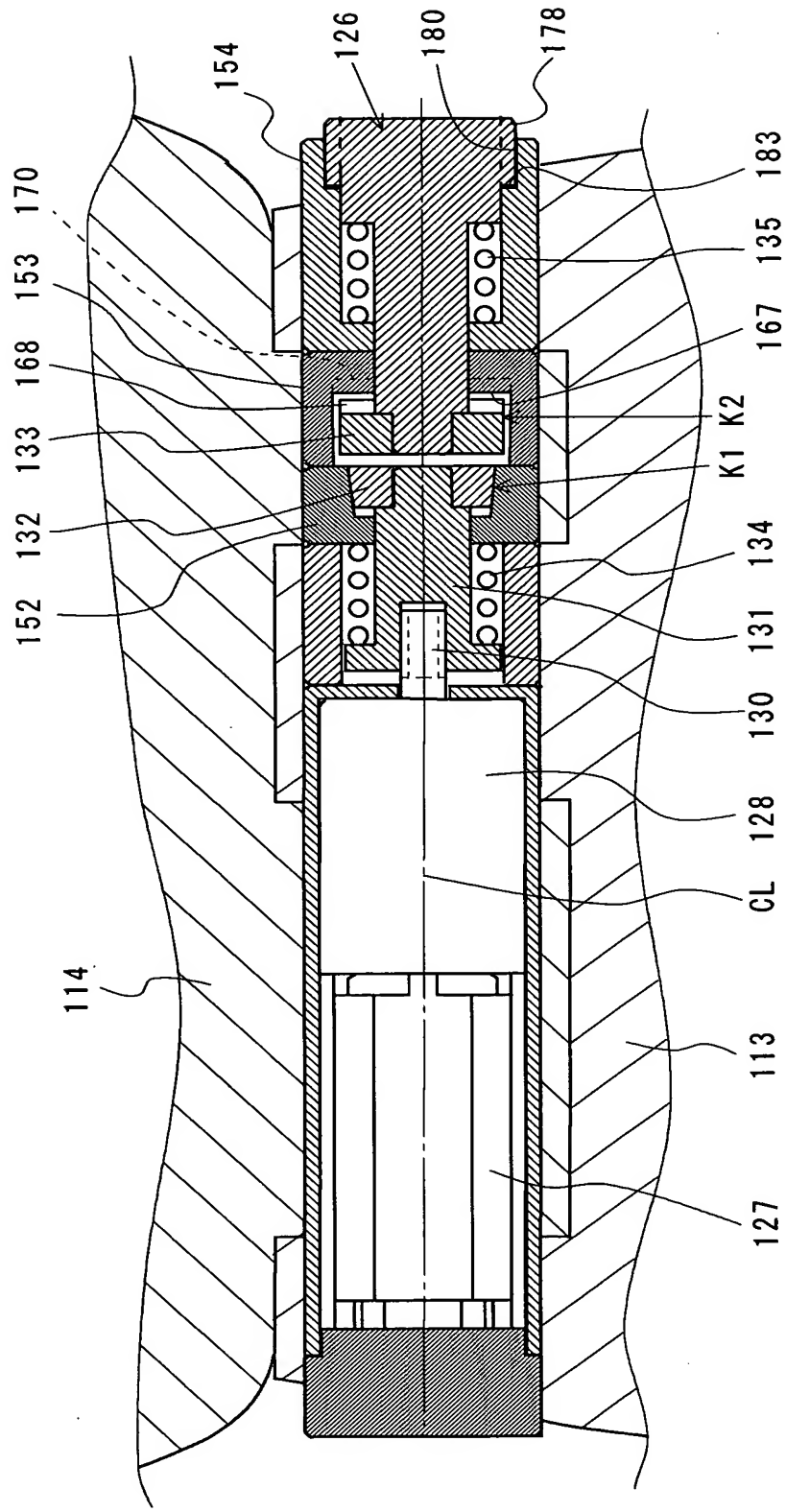


FIG. 14

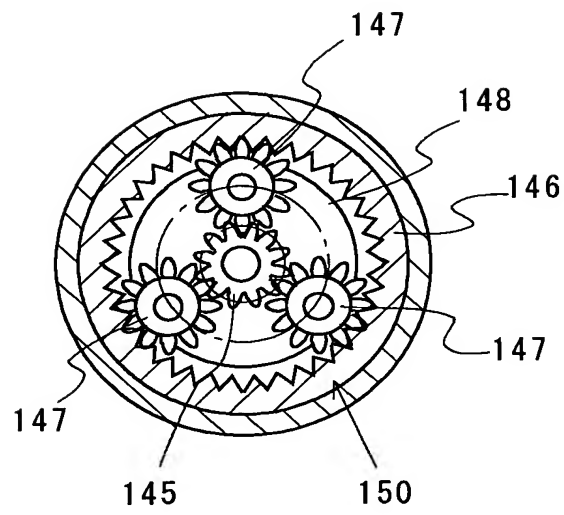


FIG. 15

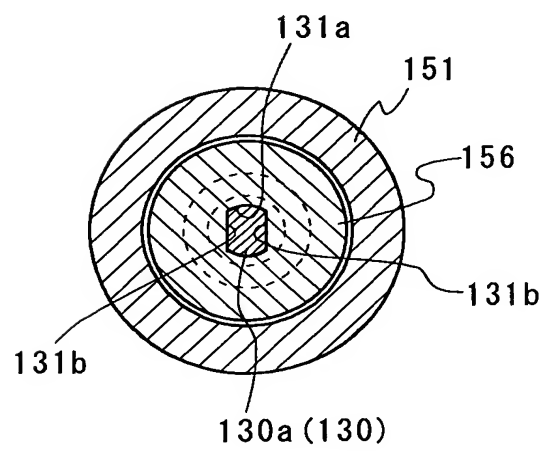


FIG. 16A

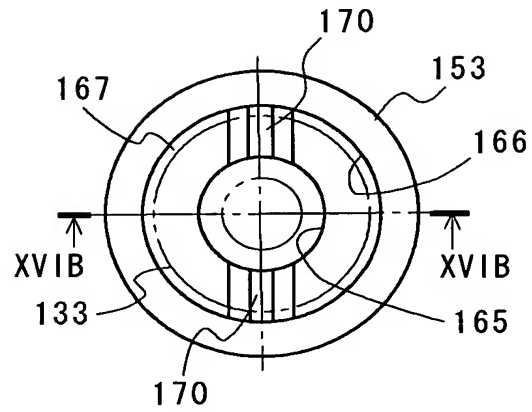


FIG. 16B

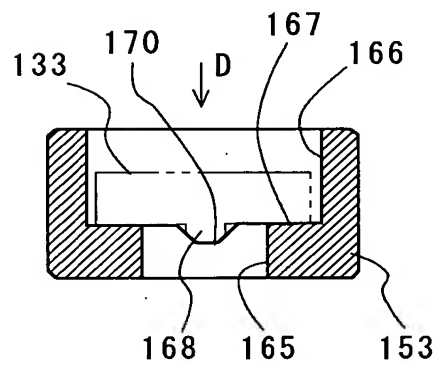


FIG. 17

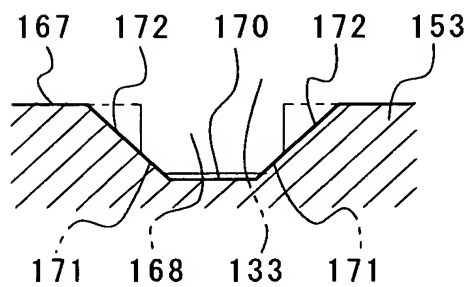


FIG. 18 is a cross-sectional view of a circular structure. It features a central core (178) surrounded by a layer (180). This is enclosed by a thick ring (181) which has a central rectangular opening (182).

